

## 4M x 16-Bit Dynamic RAM (8k, 4k & 2k Refresh, EDO-Version)

HYB 3164165AT(L) -40/-50/-60  
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### Advanced Information

- 4 194 304 words by 16-bit organization
- 0 to 70 °C operating temperature
- Hyper Page Mode - EDO - operation
- Performance:

		-40	-50	-60	
t <sub>RAC</sub>	$\overline{\text{RAS}}$ access time	40	50	60	ns
t <sub>CAC</sub>	$\overline{\text{CAS}}$ access time	10	13	15	ns
t <sub>AA</sub>	Access time from address	20	25	30	ns
t <sub>RC</sub>	Read/write cycle time	69	84	104	ns
t <sub>HPC</sub>	Hyper page mode (EDO) cycle time	16	20	25	ns

- Single + 3.3 V ( $\pm 0.3V$ ) power supply
- Low power dissipation:

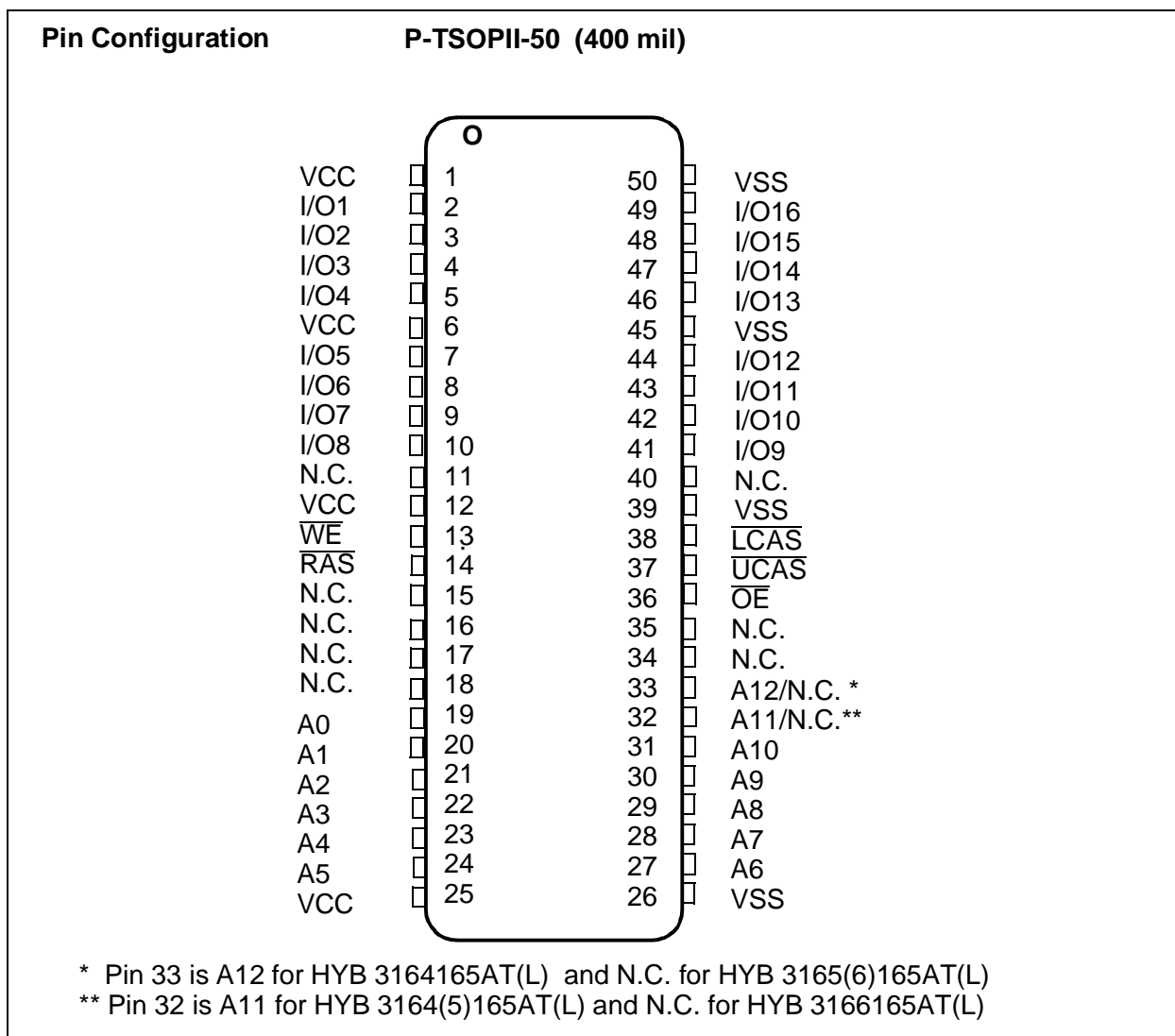
	-40	-50	-60	
HYB3166165AT(L)	1008	612	450	mW
HYB3165165AT(L)	756	504	360	mW
HYB3164165AT(L)	612	324	324	mW

- 7.2 mW standby (TTL)
- 3.24 mW standby (MOS)
- 720  $\mu\text{A}$  standby for L-version
- Read, write, read-modify-write,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh (CBR),  $\overline{\text{RAS}}$ -only refresh, hidden refresh and Self Refresh (L-version only)
- 2  $\overline{\text{CAS}}$  / 1  $\overline{\text{WE}}$  byte control
- 8192 refresh cycles/128 ms , 13 R/ 9C addresses (HYB 3164165AT)
- 4096 refresh cycles/ 64 ms , 12 R/ 10C addresses (HYB 3165165AT)
- 2048 refresh cycles/ 32 ms , 11 R/ 11C addresses (HYB 3166165AT)
- 256ms refresh period for L-versions
- Plastic Package: P-TSOP11-50 400 mil

This device is a 64 MBit dynamic RAM organized 4 194 304 x 16 bits. The device is fabricated on an advanced first generation 64Mbit 0,35 μm CMOS silicon gate process technology. The circuit and process design allow this device to achieve high performance and low power dissipation. The HYB3164(5)165AT operates with a single 3.3 +/-0.3V power supply and interfaces with either LVTTTL or LVCMOS levels. Multiplexed address inputs permit the HYB3164(5/6)165AT to be packaged in 400mil wide TSOPII-50 package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. The HYB3164(5/6)165ATL parts have a very low power „sleep mode“ supported by Self Refresh.

### Ordering Information

Type	Ordering Code	Package	Descriptions
<b>8k-refresh versions:</b>			
HYB 3164165AT-40		P-TSOPII-50 400 mil	EDO-DRAM (access time 40 ns)
HYB 3164165AT-50		P-TSOPII-50 400 mil	EDO-DRAM (access time 50 ns)
HYB 3164165AT-60		P-TSOPII-50 400 mil	EDO-DRAM (access time 60 ns)
HYB 3164165ATL-50		P-TSOPII-50 400 mil	EDO-DRAM (access time 50 ns)
HYB 3164165ATL-60		P-TSOPII-50 400 mil	EDO-DRAM (access time 60 ns)
<b>4k-refresh versions:</b>			
HYB 3165165AT-40		P-TSOPII-50 400 mil	EDO-DRAM (access time 40 ns)
HYB 3165165AT-50		P-TSOPII-50 400 mil	EDO-DRAM (access time 50 ns)
HYB 3165165AT-60		P-TSOPII-50 400 mil	EDO-DRAM (access time 60 ns)
HYB 3165165ATL-50		P-TSOPII-50 400 mil	EDO-DRAM (access time 50 ns)
HYB 3165165ATL-60		P-TSOPII-50 400 mil	EDO-DRAM (access time 60 ns)
<b>2k-refresh versions:</b>			
HYB 3166165AT-40		P-TSOPII-50 400 mil	EDO-DRAM (access time 40 ns)
HYB 3166165AT-50		P-TSOPII-50 400 mil	EDO-DRAM (access time 50 ns)
HYB 3166165AT-60		P-TSOPII-50 400 mil	EDO-DRAM (access time 60 ns)
HYB 3166165ATL-50		P-TSOPII-50 400 mil	EDO-DRAM (access time 50 ns)
HYB 3166165ATL-60		P-TSOPII-50 400 mil	EDO-DRAM (access time 60 ns)

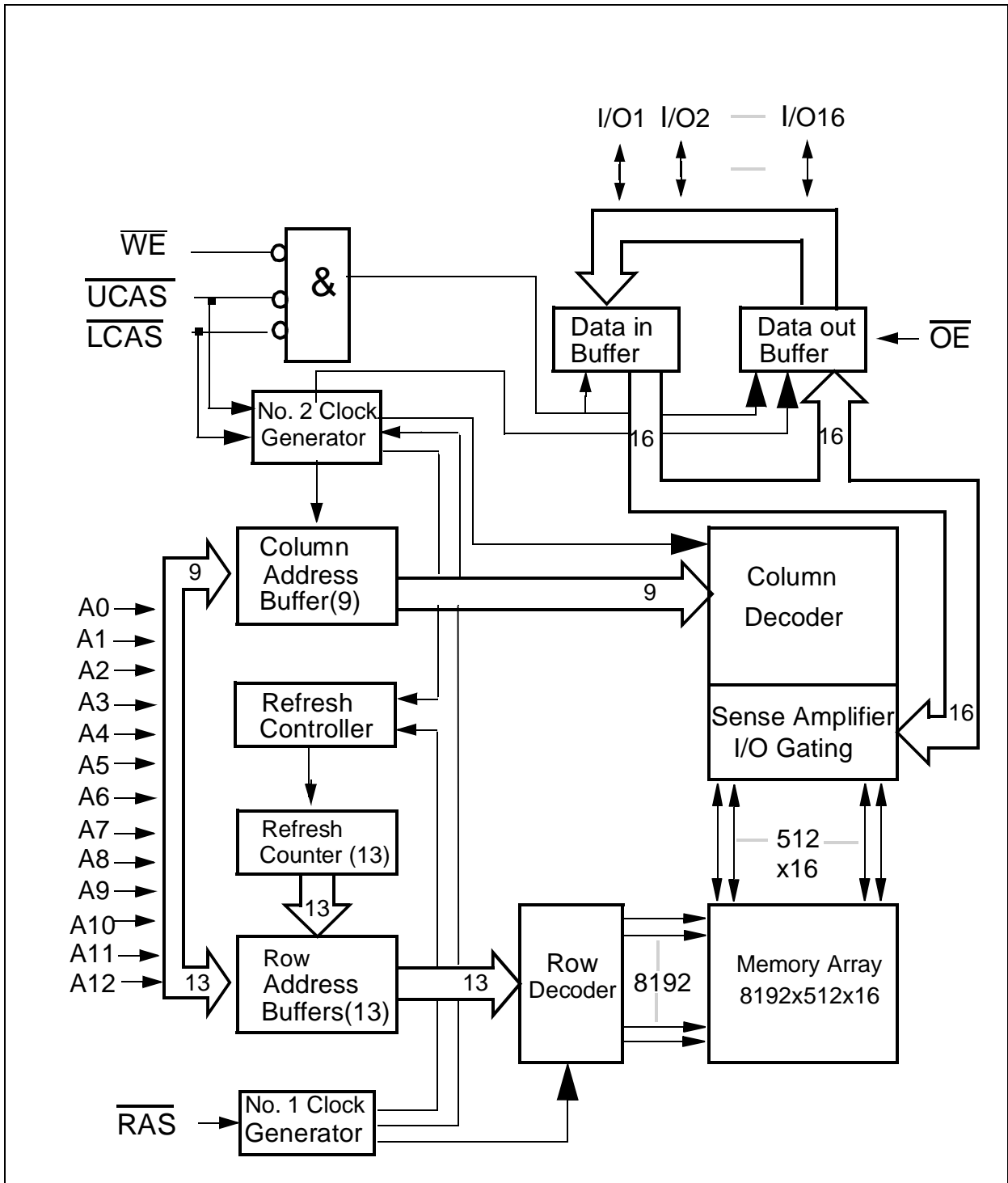


### Pin Names

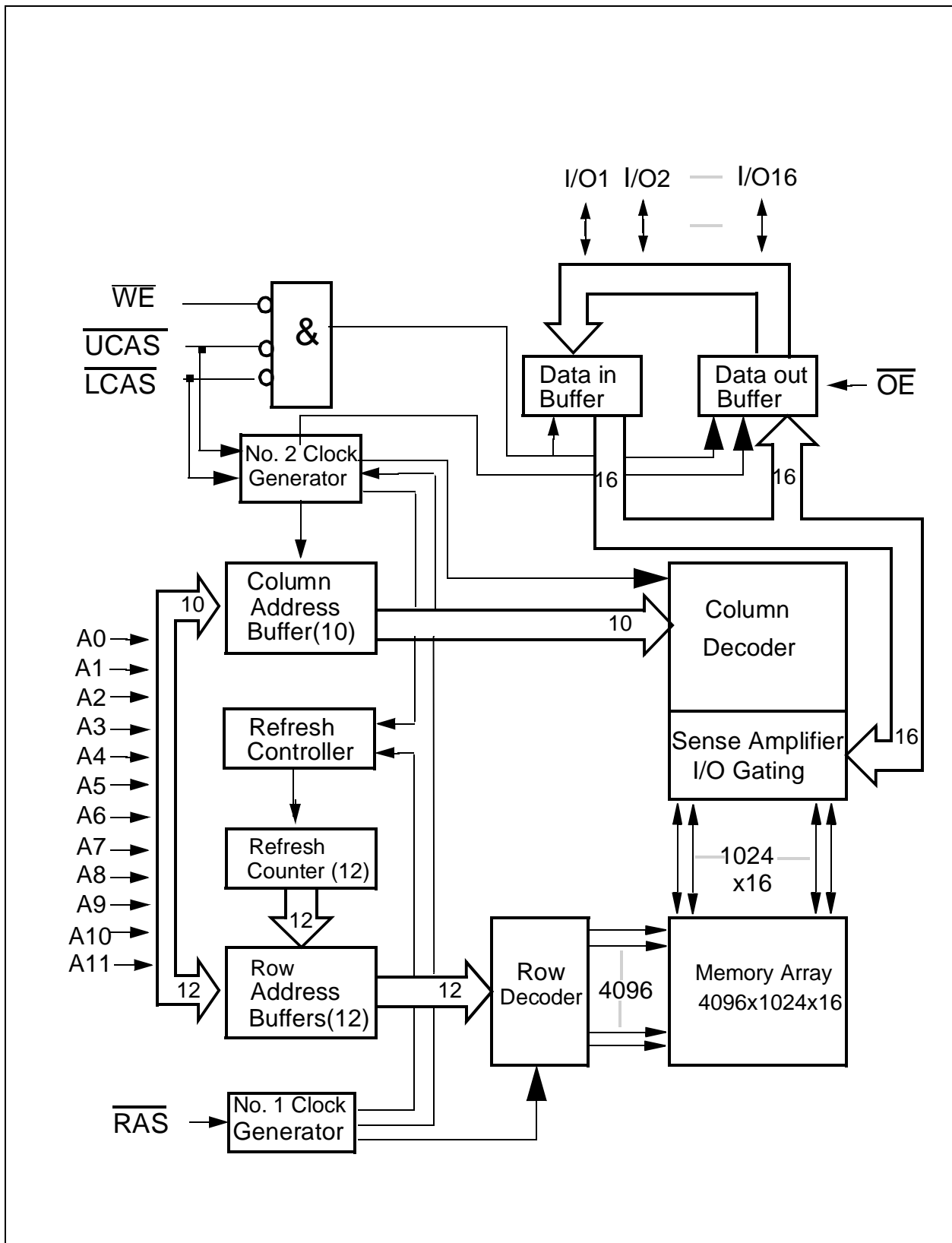
A0-A12	Address Inputs for 8k-refresh version HYB 3164165T(L)
A0-A11	Address Inputs for 4k-refresh version HYB 3165165T(L)
A0-A10	Address Inputs for 2k-refresh version HYB 3166165T(L)
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O16	Data Input/Output
$\overline{UCAS}$ , $\overline{LCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
Vcc	Power Supply ( + 3.3V)
Vss	Ground

### TRUTH TABLE

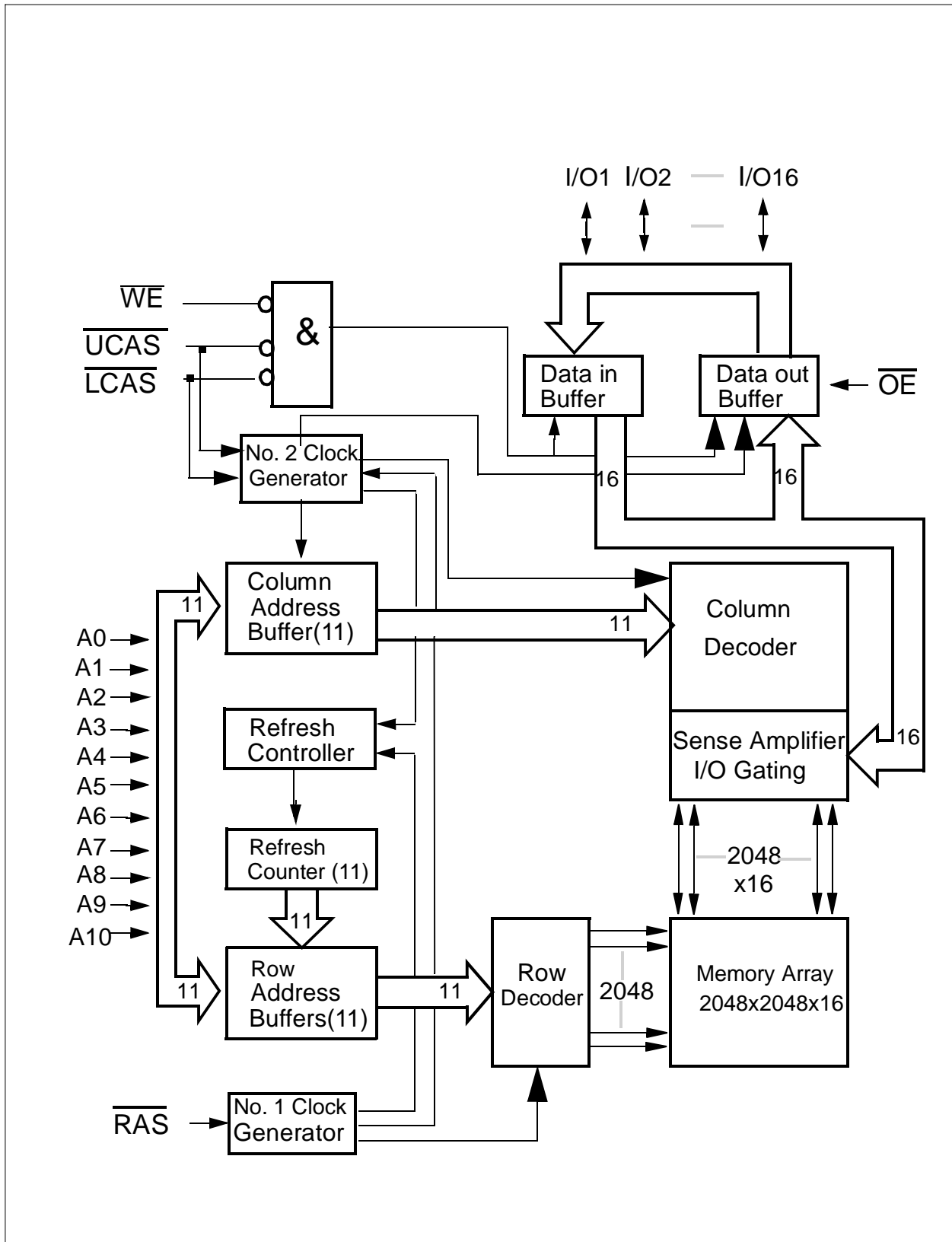
FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ROW ADD	COL ADD	I/O1- I/O16
Standby		H	H - X	H - X	X	X	X	X	High Impedance
Read:Word		L	L	H	H	L	ROW	COL	Data Out
Read:Lower Byte		L	L	H	H	L	ROW	COL	Lower Byte:Data Out Upper-Byte:High-Z
Read:Upper Byte		L	H	L	H	L	ROW	COL	Lower Byte:High-Z Upper Byte:Data Out
Write:Word (Early-Write)		L	L	L	L	X	ROW	COL	Data In
Write:Lower Byte (Early-Write)		L	L	H	L	X	ROW	COL	Lower Byte:Data Out Upper-Byte:High-Z
Write:Upper Byte (Early Write)		L	H	L	L	X	ROW	COL	Lower Byte:High-Z Upper Byte:Data Out
Read-Modify- Write		L	L	L	H - L	L - H	ROW	COL	Data Out, Data In
Hyper Page Mode Read (Word)	1st Cycle	L	H - L	H - L	H	L	ROW	COL	Data Out
Hyper Page Mode Read (Word)	2nd Cycle	L	H - L	H - L	H	L	n/a	COL	Data Out
Hyper Page Mode Early Write(Word)	1st Cycle	L	H - L	H - L	L	X	ROW	COL	Data In
Hyper Page Mode Early Write(Word)	2nd Cycle	L	H - L	H - L	L	X	n/a	COL	Data In
Hyper Page Mode RMW	1st Cycle	L	H - L	H - L	H - L	L - H	ROW	COL	Data Out, Data In
Hyper Page Mode RMW	2st Cycle	L	H - L	H - L	H - L	L - H	n/a	COL	Data Out, Data In
RAS only refresh		L	H	H	X	X	ROW	n/a	High Impedance
CAS-before-RAS refresh		H - L	L	L	H	X	X	n/a	High Impedance
Test Mode Entry		H - L	L	L	L	X	X	n/a	High Impedance
Hidden Refresh (Read)		L-H- L	L	L	H	L	ROW	COL	Data Out
Hidden Refresh (Write)		L-H- L	L	L	L	X	ROW	COL	Data In
Self Refresh (L-version only)		H-L	L	H	X	X	X	X	High Impedance



Block Diagram for HYB 3164165AT(L)



**Block Diagram for HYB 3165165AT(L)**



Block Diagram for HYB3166165AT(L)

### Absolute Maximum Ratings

Operating temperature range.....	0 to 70 °C
Storage temperature range.....	- 55 to 150 °C
Input/output voltage.....	-0.5 to min (V <sub>CC</sub> +0.5,4.6) V
Power supply voltage.....	-0.5V to 4.6 V
Power dissipation.....	1.3 W
Data out current (short circuit).....	50 mA

### Note

Stresses above those listed under „Absolute Maximum Ratings“ may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

### DC Characteristics

T<sub>A</sub> = 0 to 70 °C, V<sub>SS</sub> = 0 V, V<sub>CC</sub> = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	V <sub>IH</sub>	2.0	V <sub>CC</sub> +0.3	V	1)
Input low voltage	V <sub>IL</sub>	- 0.3	0.8	V	1)
Output high voltage (LVTTTL) Output „H“ level voltage (I <sub>out</sub> = -2mA)	V <sub>OH</sub>	2.4	-	V	
Output low voltage (LVTTTL) Output „L“ level voltage (I <sub>out</sub> = +2mA)	V <sub>OL</sub>	-	0.4	V	
Output high voltage (LVCMOS) Output „H“ level voltage (I <sub>out</sub> = -100uA)	V <sub>OH</sub>	V <sub>CC</sub> -0.2	-	V	
Output low voltage (LVCMOS) Output „L“ level voltage (I <sub>out</sub> = +100uA)	V <sub>OL</sub>	-	0.2	V	
Input leakage current,any input (0 V < V <sub>in</sub> < V <sub>CC</sub> , all other pins = 0 V)	I <sub>I(L)</sub>	- 2	2	μA	
Output leakage current (DO is disabled, 0 V < V <sub>out</sub> < V <sub>CC</sub> )	I <sub>O(L)</sub>	- 2	2	μA	



### DC-Characteristics (cont'd)

$T_A = 0$  to  $70$  °C,  $V_{SS} = 0$  V,  $V_{CC} = 3.3$  V  $\pm$  0.3 V

Parameter	Symbol	refresh version			Unit	Note
		2k	4k	8k		
Operating Current -40 ns version -50 ns version -60 ns version ( $\overline{RAS}$ , $\overline{CAS}$ , address cycling: tRC = tRC min.)	$I_{CC1}$	280 230 185	170 140 115	125 100 85	mA mA mA	2) 3) 4)
Standby Current (RAS=CAS= Vih)	$I_{CC2}$	2	2	2	mA	–
$\overline{RAS}$ Only Refresh Current: -40 ns version -50 ns version -60 ns version (RAS cycling: CAS = VIH: tRC = tRC min.)	$I_{CC3}$	280 230 185	170 140 115	125 100 84	mA mA mA	2) 4)
Hyper Page Mode (EDO) Current: -40 ns version -50 ns version -60 ns version ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , address cycling: tHPC=tHPC min.)	$I_{CC4}$	140 105 85	140 105 85	140 105 85	mA mA mA	2) 3) 4)
Standby Current (RAS=CAS= Vcc-0.2V)	$I_{CC5}$	900	900	900	$\mu$ A	–
Standby Current (L-Version) ( $\overline{RAS}=\overline{CAS}= V_{cc}-0.2V$ )	$I_{CC5}$	200	200	200	$\mu$ A	–
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current -40 ns version -50 ns version -60 ns version ( $\overline{RAS}$ , $\overline{CAS}$ cycling: tRC = tRC min.)	$I_{CC6}$	280 230 185	170 140 115	170 140 115	mA mA mA	2) 4)
Self Refresh Current (L-version only) (CBR cycle with tRAS>TRASSmin, $\overline{CAS}$ held low, $\overline{WE} = V_{cc}-0.2V$ , Address and Din= $V_{cc}-0.2V$ or 0.2V)	$I_{CC7}$	400	400	400	$\mu$ A	

### Capacitance

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $f = 1$  MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11,A12)	$C_{I1}$	–	5	pF
Input capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , $\overline{OE}$ )	$C_{I2}$	–	7	pF
I/O capacitance (I/O1-I/O16)	$C_{I0}$	–	7	pF

### AC Characteristics <sup>5)6)</sup>

AC64-2E

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3V,  $t_T = 2$  ns

Parameter	Symbol	Limit Values						Unit	Note
		- 40		- 50		- 60			
		min.	max.	min.	max.	min.	max.		

### Common Parameters

Random read or write cycle time	$t_{RC}$	69	–	84	–	104	–	ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	40	100k	50	100k	60	100k	ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	6	100k	8	100k	10	100k	ns	
$\overline{RAS}$ precharge time	$t_{RP}$	25	–	30	–	40	–	ns	
$\overline{CAS}$ precharge time	$t_{CP}$	6	–	8	–	10	–	ns	
Row address setup time	$t_{ASR}$	0	–	0	–	0	–	ns	
Row address hold time	$t_{RAH}$	5	–	7	–	10	–	ns	
Column address setup time	$t_{ASC}$	0	–	0	–	0	–	ns	
Column address hold time	$t_{CAH}$	5	–	7	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	9	30	11	37	14	45	ns	
$\overline{RAS}$ to column address delay time	$t_{RAD}$	7	20	9	25	12	30	ns	
$\overline{RAS}$ hold time	$t_{RSH}$	6	–	8	–	10	–	ns	
$\overline{CAS}$ hold time	$t_{CSH}$	32	–	40	–	48	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	–	5	–	5	–	ns	
Transition time (rise and fall)	$t_T$	1	50	1	50	1	50	ns	7
Refresh period for 8k-refresh-version	$t_{REF}$	–	128	–	128	–	128	ms	
Refresh period for 4k-refresh version	$t_{REF}$	–	64	–	64	–	64	ms	
Refresh period for L-versions	$t_{REF}$	–	256	–	256	–	256	ms	

### Read Cycle

Access time from $\overline{RAS}$	$t_{RAC}$	–	40	–	50	–	60	ns	8, 9
Access time from $\overline{CAS}$	$t_{CAC}$	–	10	–	13	–	15	ns	8, 9
Access time from column address	$t_{AA}$	–	20	–	25	–	30	ns	8,10
$\overline{OE}$ access time	$t_{OEA}$	–	10	–	13	–	15	ns	
Column address to $\overline{RAS}$ lead time	$t_{RAL}$	20	–	25	–	30	–	ns	
Read command setup time	$t_{RCS}$	0	–	0	–	0	–	ns	
Read command hold time	$t_{RCH}$	0	–	0	–	0	–	ns	11

### AC Characteristics *(cont'd)* <sup>5)6)</sup>

AC64-2E

 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}, V_{CC} = 3.3 \text{ V} \pm 0.3\text{V}, t_T = 2 \text{ ns}$ 

Parameter	Symbol	Limit Values						Unit	Note
		- 40		- 50		- 60			
		min.	max.	min.	max.	min.	max.		
Read command hold time referenced to $\overline{\text{RAS}}$	$t_{RRH}$	0	–	0	–	0	–	ns	11
$\overline{\text{CAS}}$ to output in low-Z	$t_{CLZ}$	0	–	0	–	0	–	ns	8
Output buffer turn-off delay	$t_{OFF}$	0	10	0	13	0	15	ns	12
Output buffer turn-off delay from $\overline{\text{OE}}$	$t_{OEZ}$	0	10	0	13	0	15	ns	12
Data to $\overline{\text{CAS}}$ low delay	$t_{DZC}$	0	–	0	–	0	–	ns	13
Data to $\overline{\text{OE}}$ low delay	$t_{DZO}$	0	–	0	–	0	–	ns	13
$\overline{\text{CAS}}$ high to data delay	$t_{CDD}$	10	–	13	–	15	–	ns	14
$\overline{\text{OE}}$ high to data delay	$t_{ODD}$	10	–	13	–	15	–	ns	14

### Write Cycle

Write command hold time	$t_{WCH}$	5	–	7	–	10	–	ns	
Write command pulse width	$t_{WP}$	5	–	7	–	10	–	ns	
Write command setup time	$t_{WCS}$	0	–	0	–	0	–	ns	15
Write command to $\overline{\text{RAS}}$ lead time	$t_{RWL}$	6	–	8	–	10	–	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{CWL}$	6	–	8	–	10	–	ns	
Data setup time	$t_{DS}$	0	–	0	–	0	–	ns	16
Data hold time	$t_{DH}$	5	–	7	–	10	–	ns	16

### Read-modify-Write Cycle

Read-write cycle time	$t_{RWC}$	89	–	109	–	133	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	$t_{RWD}$	52	–	65	–	77	–	ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	$t_{CWD}$	22	–	28	–	32	–	ns	15
Column address to $\overline{\text{WE}}$ delay time	$t_{AWD}$	32	–	40	–	47	–	ns	15
$\overline{\text{OE}}$ command hold time	$t_{OEHL}$	5	–	7	–	10	–	ns	

### Hyper Page Mode (EDO) Cycle

Hyper page mode (EDO) cycle time	$t_{HPC}$	16	–	20	–	24	–	ns	
Access time from $\overline{\text{CAS}}$ precharge	$t_{CPA}$	–	22	–	27	–	32	ns	7
Output data hold time	$t_{COH}$	3	–	5	–	5	–	ns	

**AC Characteristics** (cont'd) <sup>5)6)</sup>

AC64-2E

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$ ,  $V_{CC} = 3.3 \text{ V} \pm 0.3\text{V}$ ,  $t_T = 2 \text{ ns}$

Parameter	Symbol	Limit Values						Unit	Note
		- 40		- 50		- 60			
		min.	max.	min.	max.	min.	max.		
$\overline{\text{RAS}}$ pulse width in hyper page mode	$t_{\text{RAS}}$	40	200k	50	200k	60	200k	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ Delay	$t_{\text{RHPC}}$	22	–	27	–	32	–	ns	
$\overline{\text{OE}}$ pulse width	$t_{\text{OEP}}$	5	–	5	–	5	–	ns	
$\overline{\text{OE}}$ hold time from $\overline{\text{CAS}}$ high	$t_{\text{OEHC}}$	5	–	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{\text{WE}}$	$t_{\text{WEZ}}$	0	10	0	13	0	15	ns	
$\overline{\text{OE}}$ setup time prior to $\overline{\text{CAS}}$	$t_{\text{OES}}$	5	–	5	–	5	–	ns	

**Hyper Page Mode (EDO) Read-modify-Write Cycle**

Hyper page mode (EDO) read-write cycle time	$t_{\text{PRWC}}$	44	–	54	–	63	–	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$	$t_{\text{CPWD}}$	34	–	42	–	49	–	ns	

**$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Refresh Cycle**

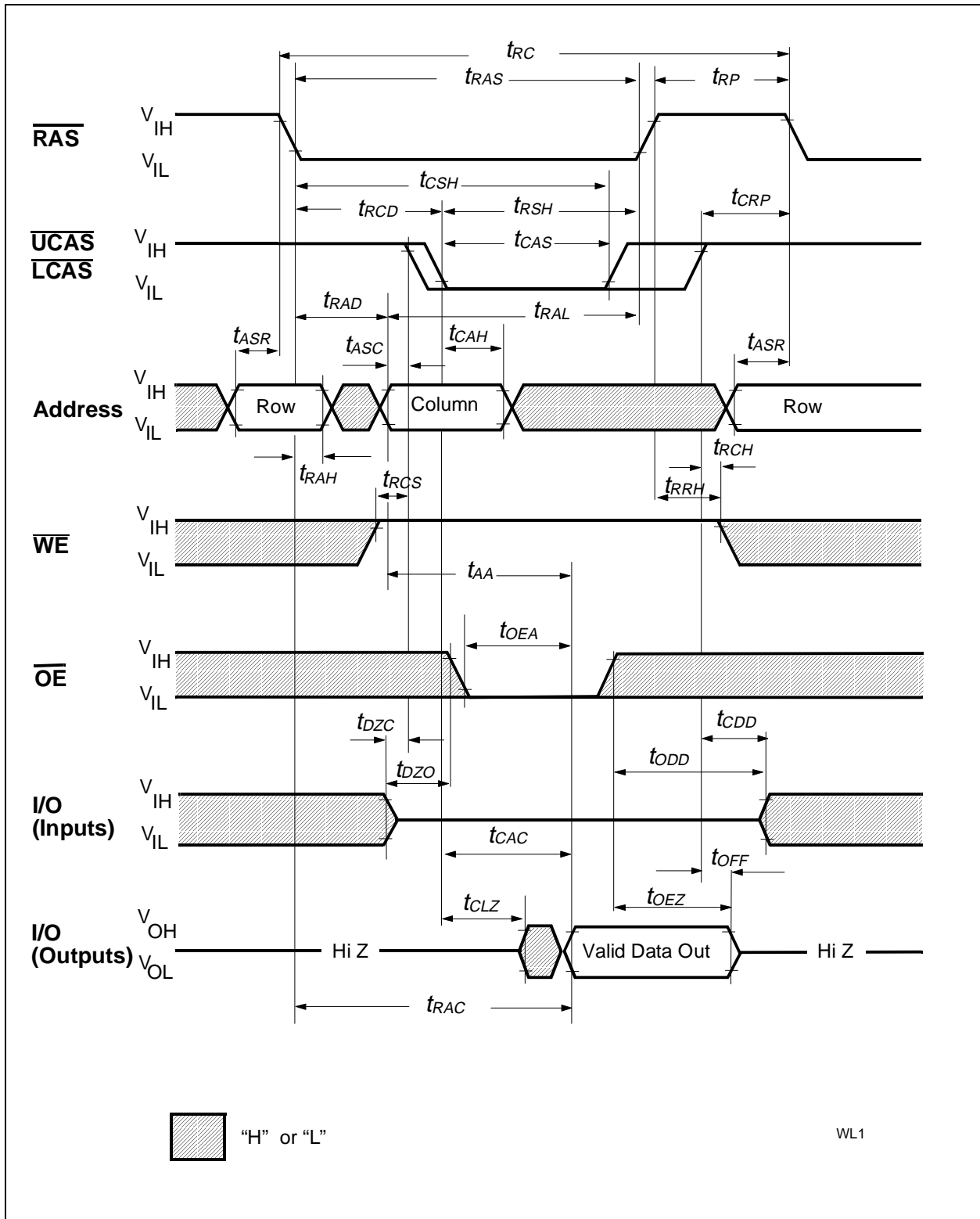
$\overline{\text{CAS}}$ setup time	$t_{\text{CSR}}$	5	–	5	–	5	–	ns	
$\overline{\text{CAS}}$ hold time	$t_{\text{CHR}}$	5	–	5	–	10	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	$t_{\text{RPC}}$	5	–	5	–	5	–	ns	
Write to $\overline{\text{RAS}}$ precharge time	$t_{\text{WRP}}$	5	–	5	–	10	–	ns	
Write hold time referenced to $\overline{\text{RAS}}$	$t_{\text{WRH}}$	5	–	5	–	10	–	ns	

**Self Refresh Cycle (L-versions only)**

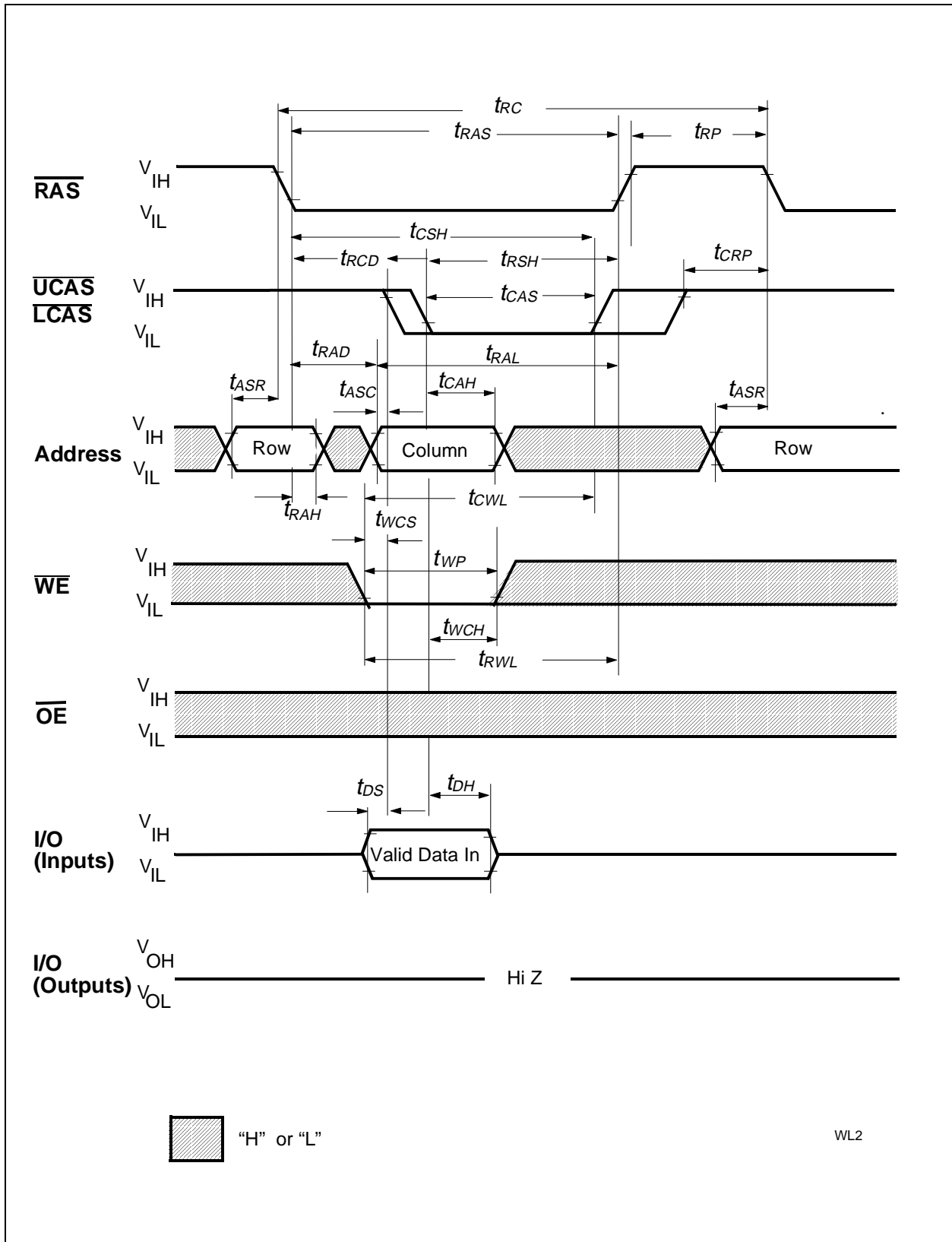
$\overline{\text{RAS}}$ pulse width	$t_{\text{RASS}}$	100k		100k	–	100k	–	ns	17
$\overline{\text{RAS}}$ precharge time	$t_{\text{RPS}}$	69	–	84	–	104	–	ns	17
$\overline{\text{CAS}}$ hold time	$t_{\text{CHS}}$	-50	–	-50	–	-50	–	ns	17

**Notes:**

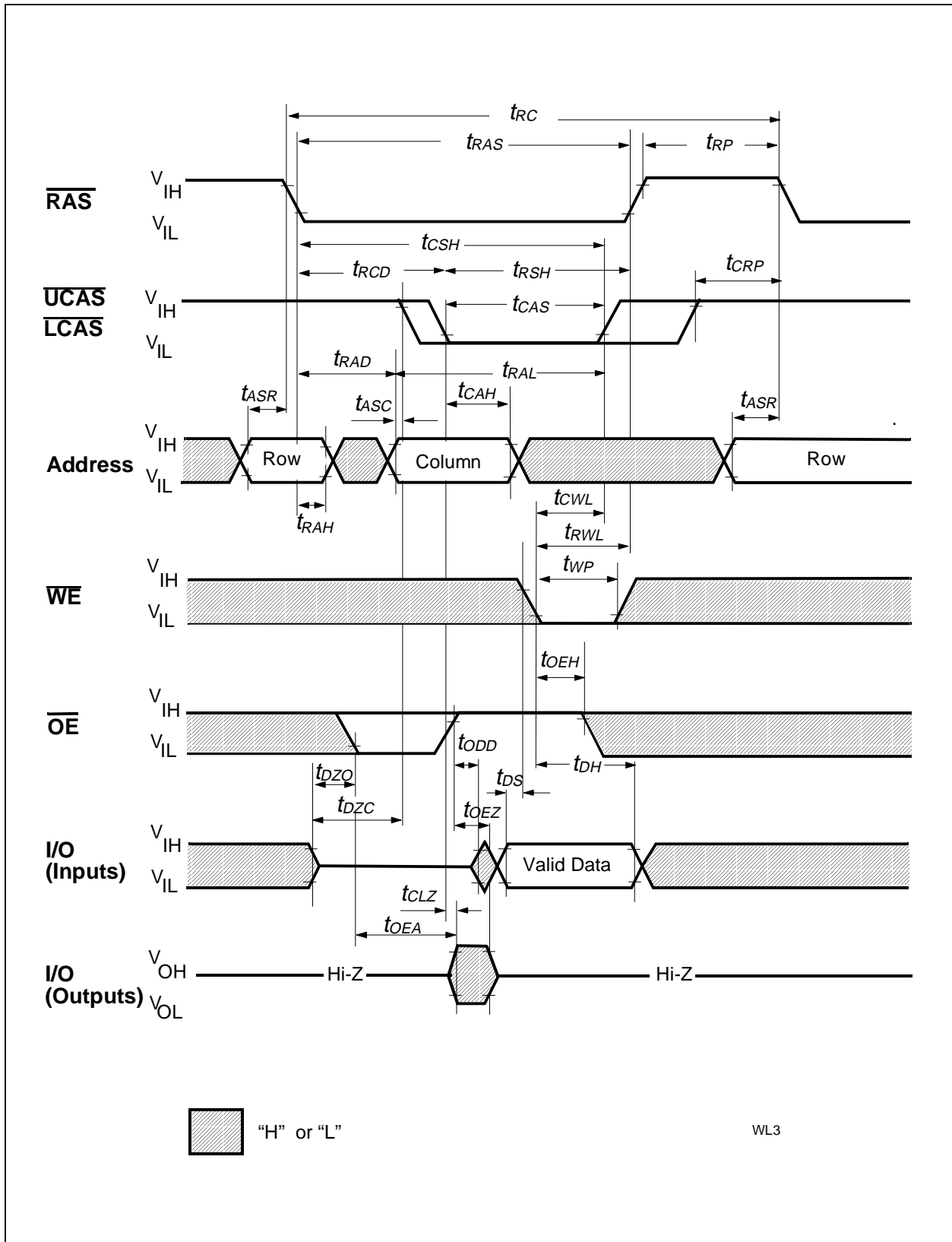
- 1) All voltages are referenced to VSS.  
Vih may overshoot to Vcc + 2.0 V for pulse widths of < 4ns with 3.3V. Vil may undershoot to -2.0V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.
- 2) ICC1, ICC3, ICC4 and ICC6 and ICC7 depend on cycle rate.
- 3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.
- 4) Address can be changed once or less while  $\overline{RAS} = V_{il}$ . In the case of ICC4 it can be changed once or less during a Hyper page mode cycle ( thpc).
- 5) An initial pause of 100  $\mu$ s is required after power-up followed by 8  $\overline{RAS}$ -only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
- 6) AC measurements assume  $t_T = 2$  ns.
- 7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL.
- 8) Measured with the specified current load and 100 pF at Voh = 2.0 V and Vol = 0.8 V.
- 9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.
- 10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.
- 11) Either tRCH or tRRH must be satisfied for a read cycle.
- 12) tOFF (max.) and tOEZ (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
- 13) Either tDZC or tDZO must be satisfied.
- 14) Either tCDD or tODD must be satisfied.
- 15) tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $tWCS > tWCS$  (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if  $tRWD > tRWD$  (min.),  $tCWD > tCWD$  (min.),  $tAWD > tAWD$  (min.) and  $tCPWD > tCPWD$  (min.) , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
- 16) These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WRITE}$  leading edge in Read-Modify-Write cycles.
- 17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:  
If row addresses are being refresh in an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediatly after exit from Self Refresh.  
If row addresses are being refresh in any other manner (ROR - Distributed/Burst or CBR-Burst) over the refresh interval, then a full set of row refreshed must be performed immediately before entry to and immediatey after exit from Self Refresh



Read Cycle



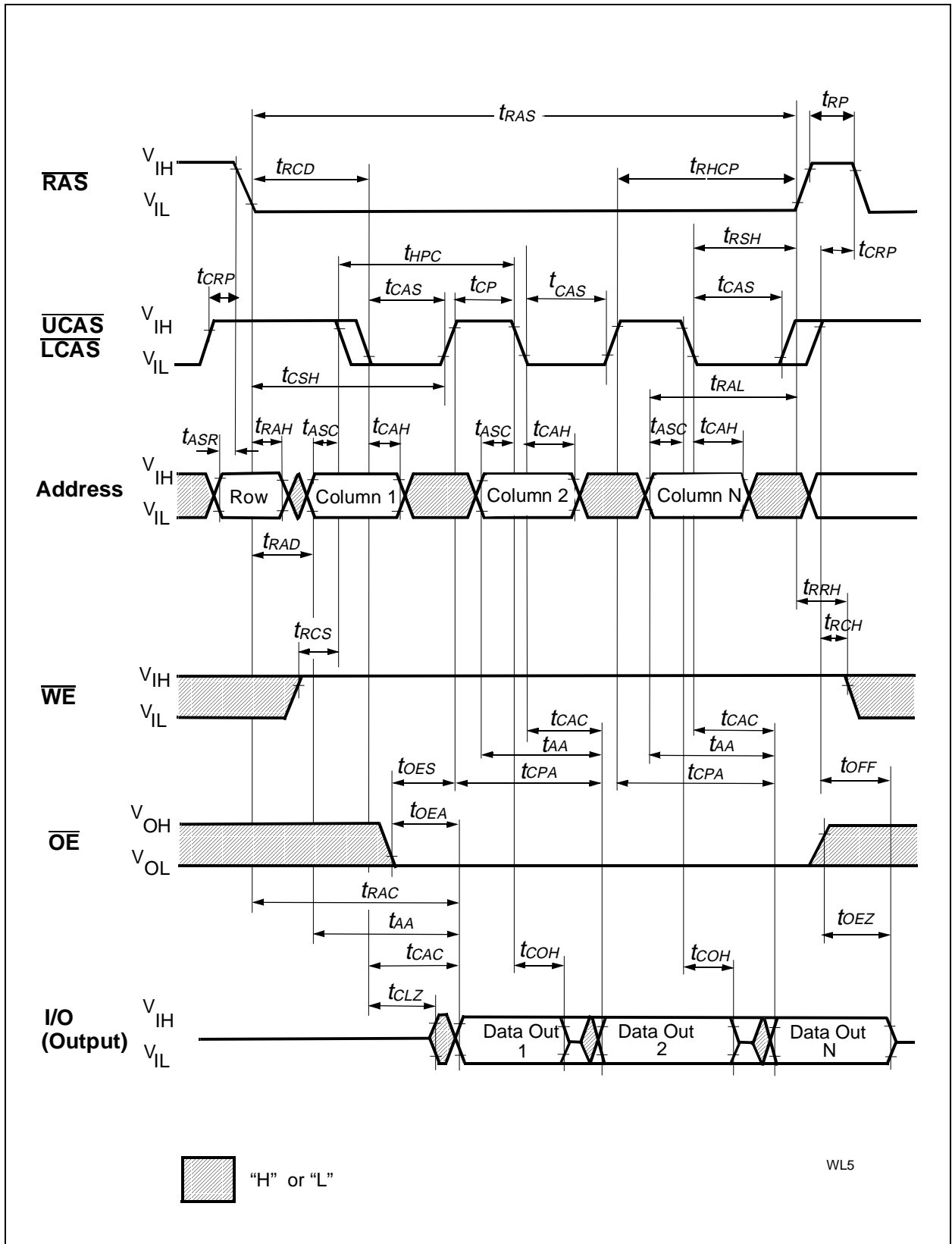
Write Cycle (Early Write)



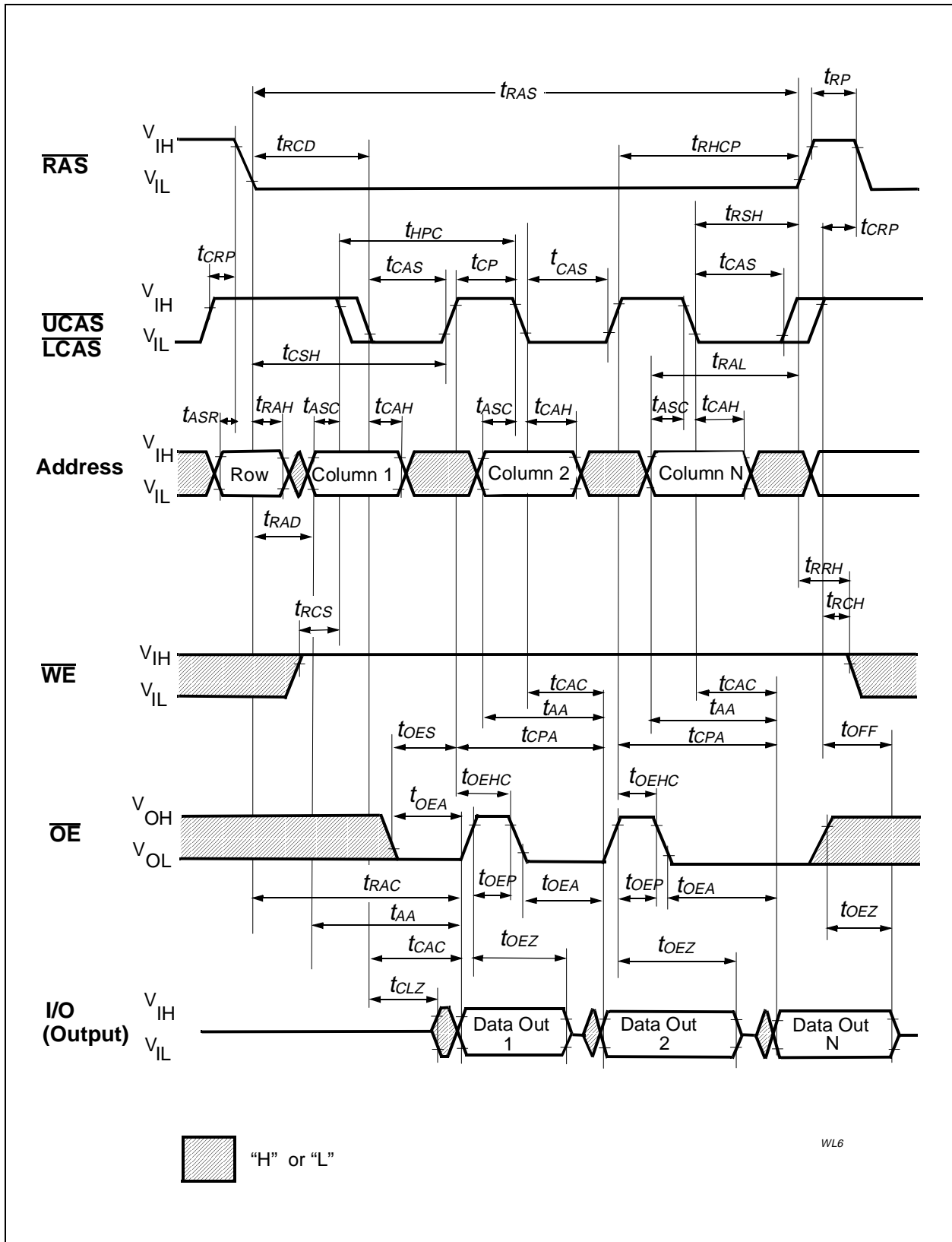
Write Cycle ( $\overline{OE}$  Controlled Write)



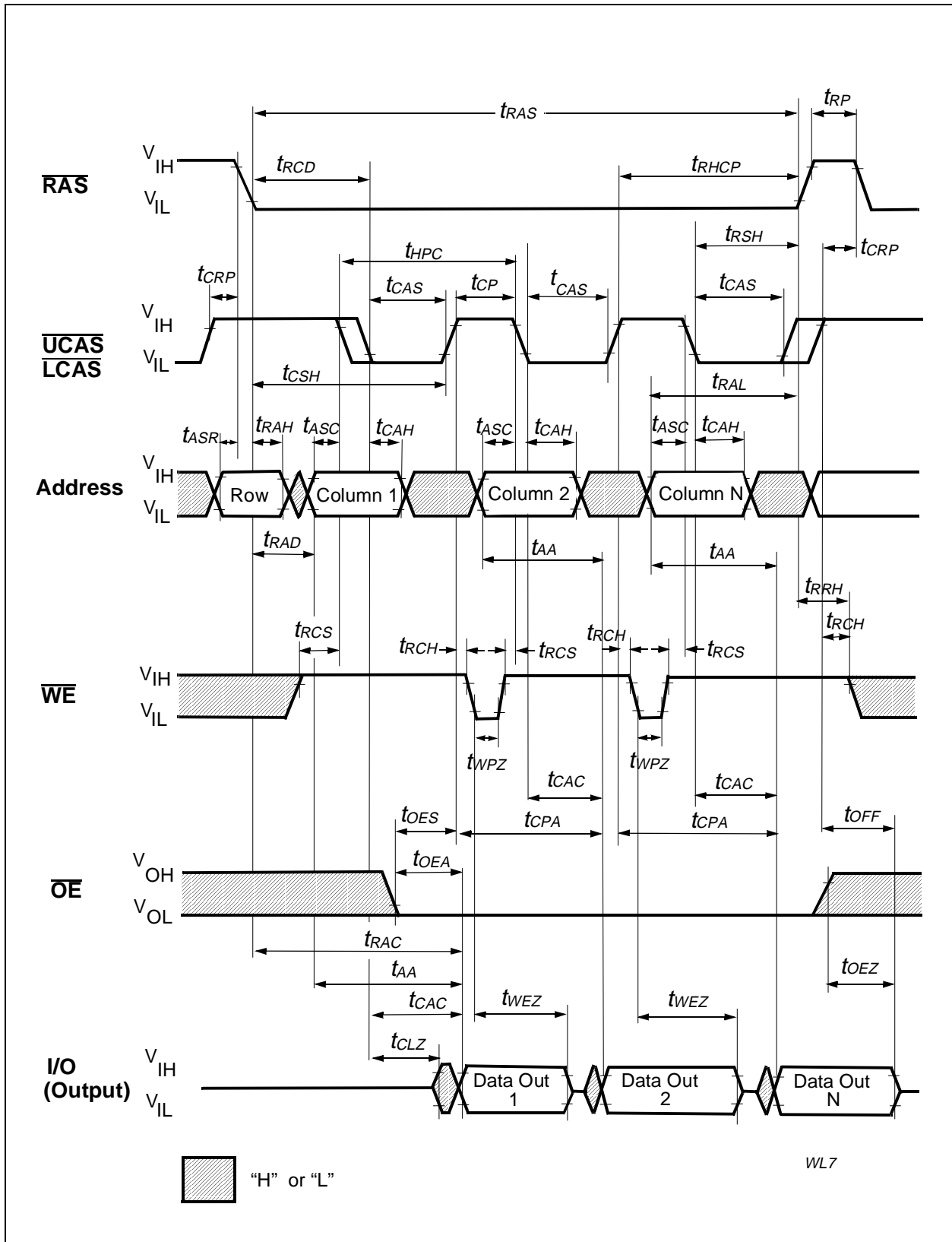




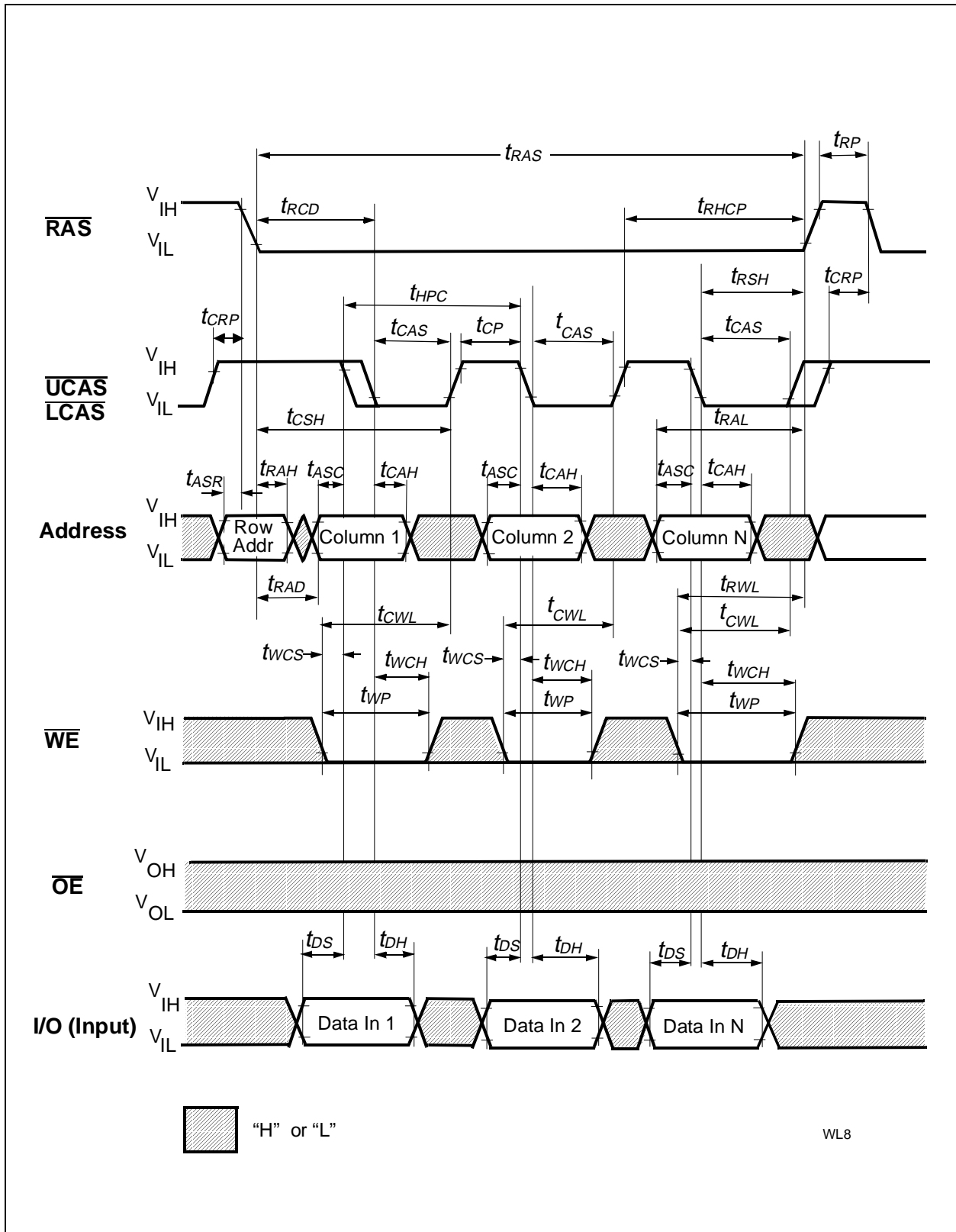
Hyper Page Mode (EDO) Read Cycle



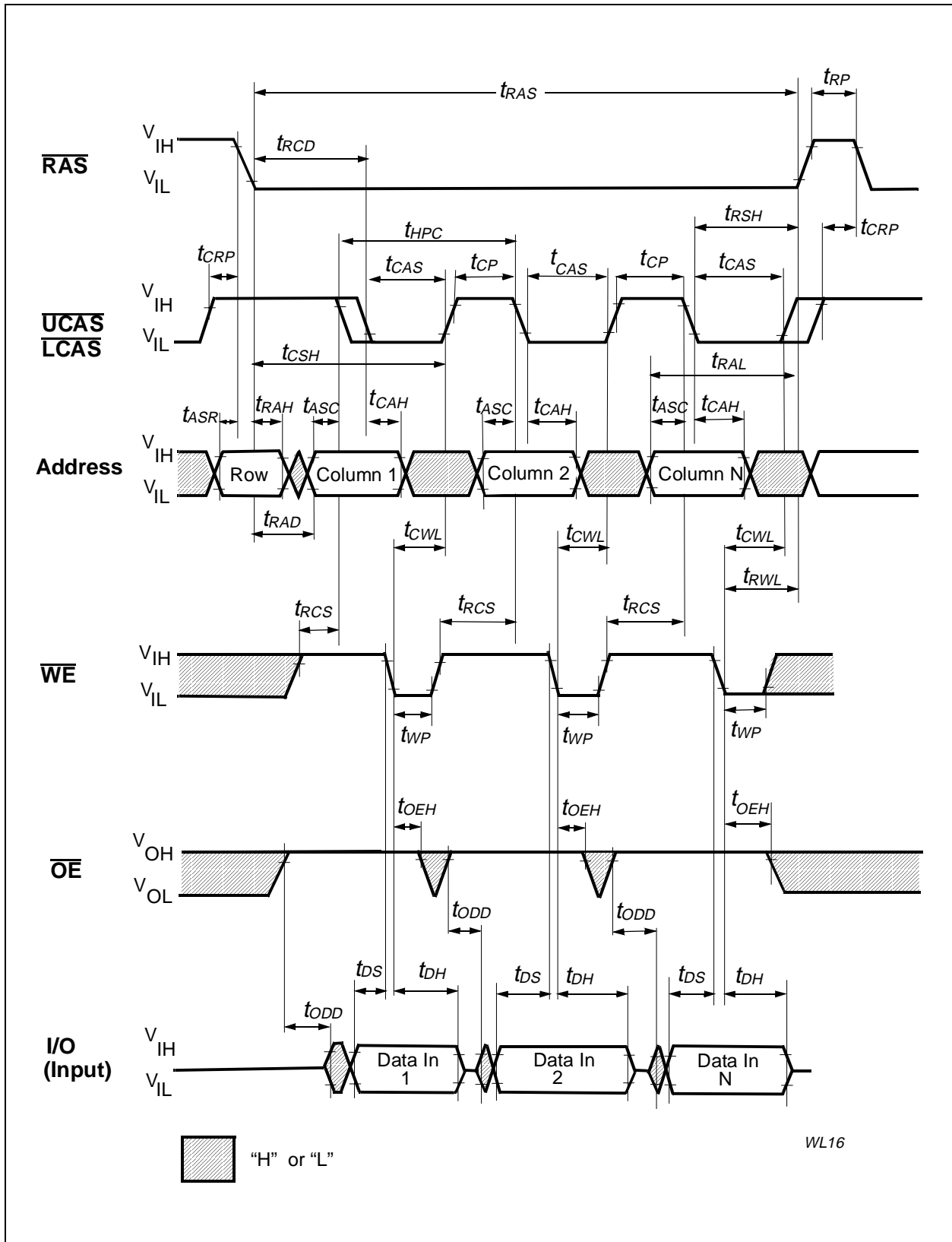
Hyper Page Mode (EDO) Read Cycle ( $\overline{OE}$  Control)



Hyper Page Mode (EDO) Read Cycle ( $\overline{WE}$  Control)

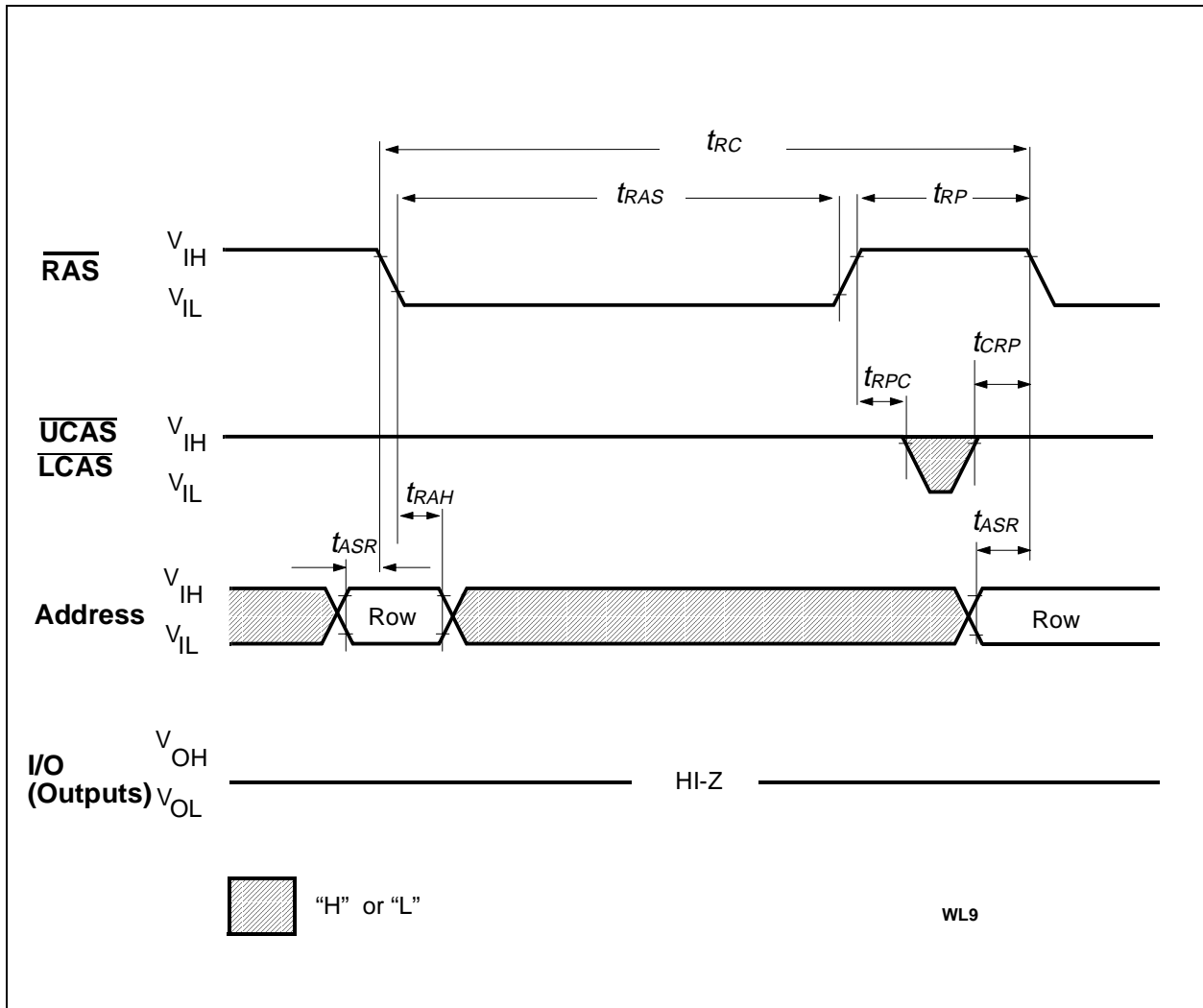


Hyper Page Mode (EDO) Early Write Cycle



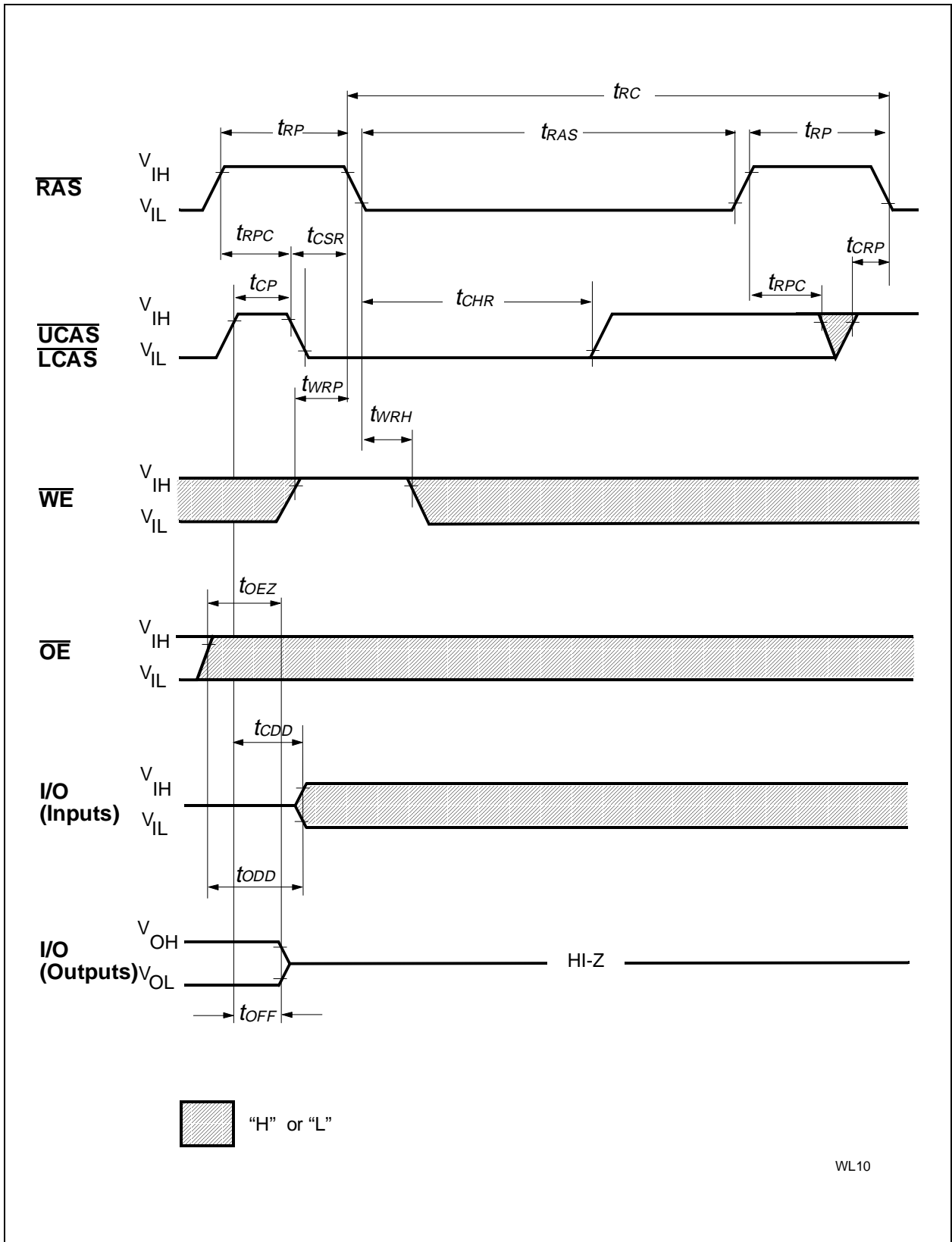
Hyper Page Mode (EDO) Late Write Cycle



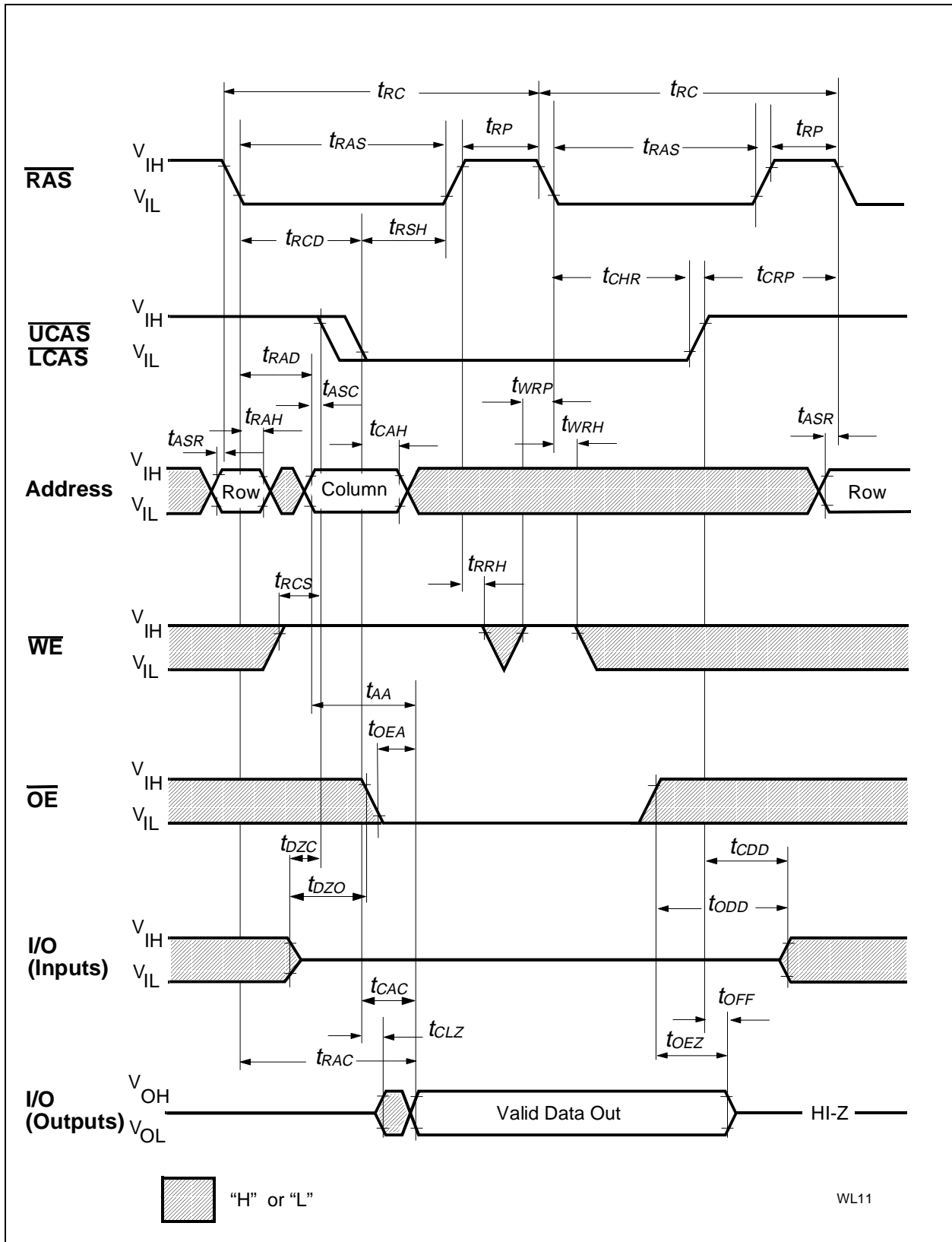


RAS Only Refresh Cycle

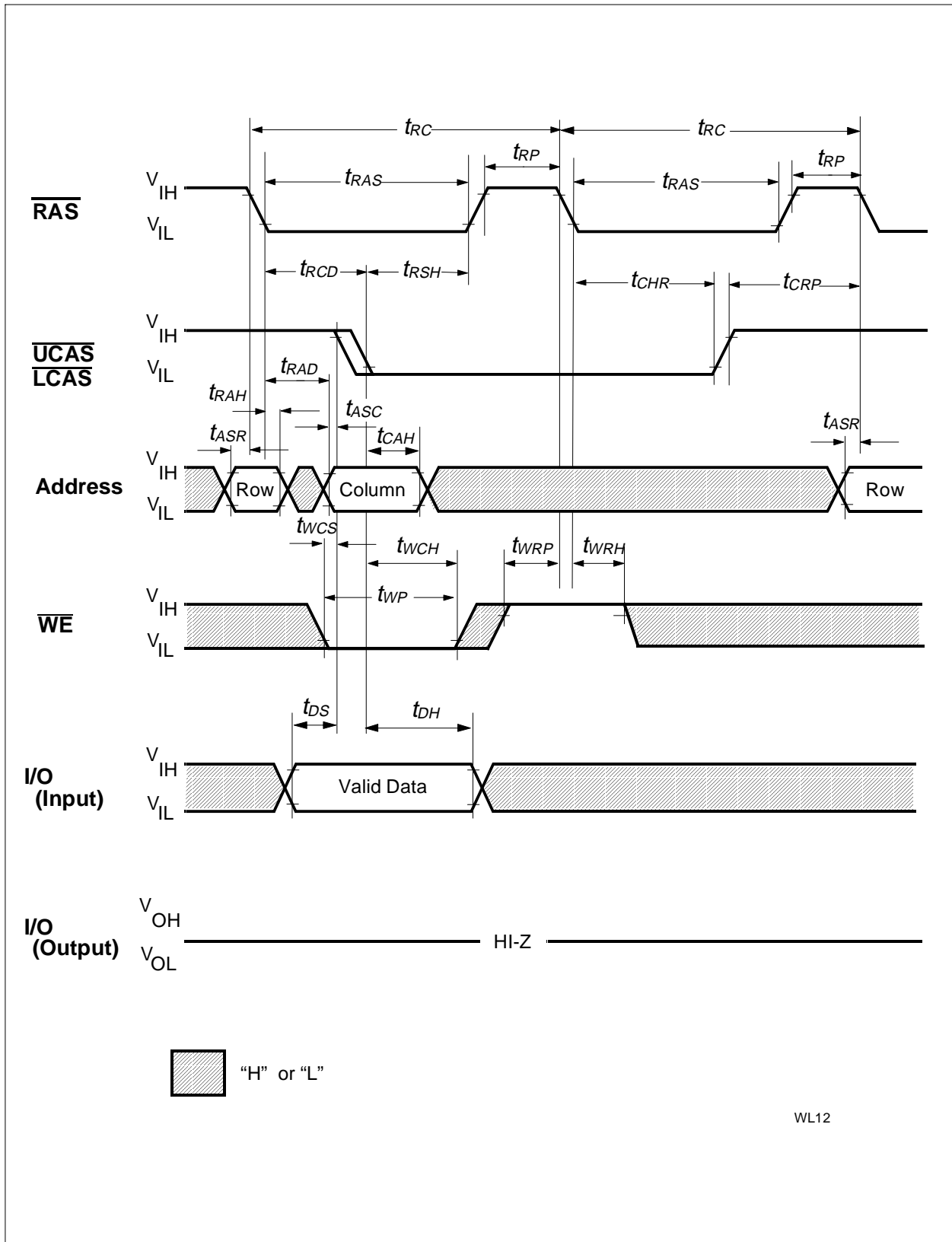




CAS-before-RAS Refresh Cycle

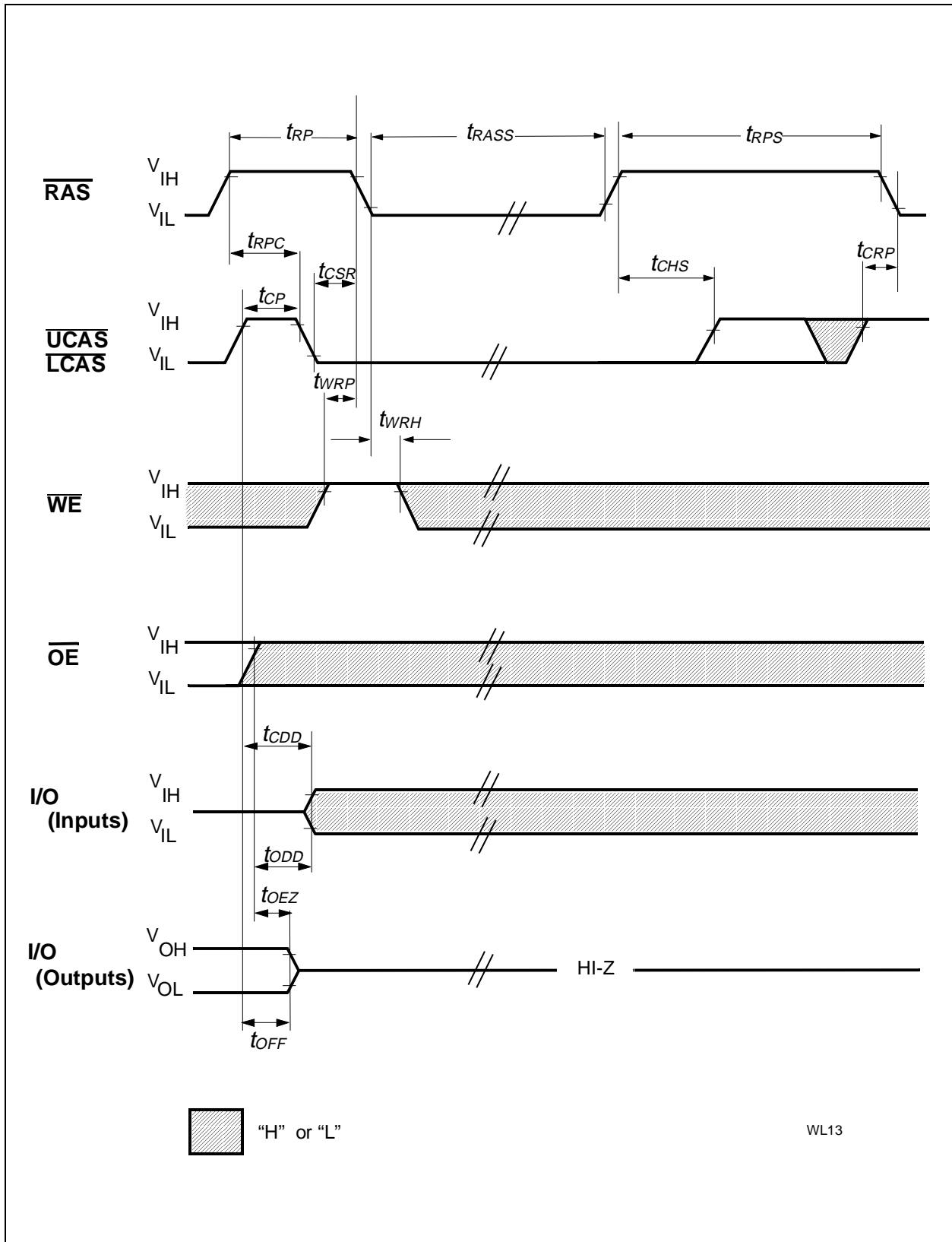


Hidden Refresh Read Cycle



WL12

Hidden Refresh Early Write Cycle

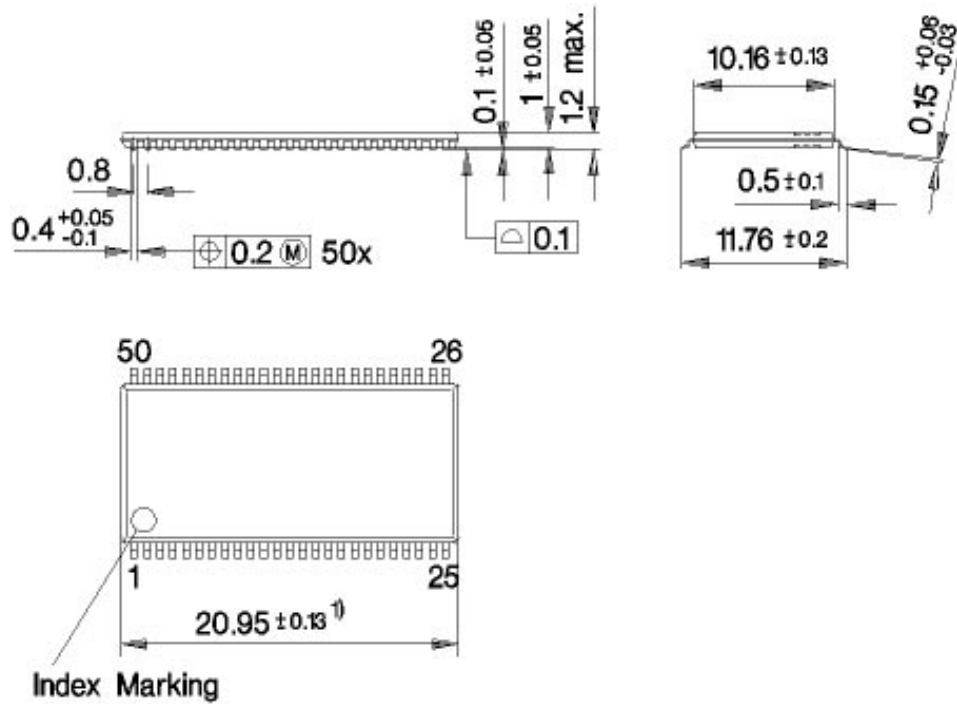


Self Refresh (Sleep Mode)

**Package Outlines**

**Plastic Package P-TSOPII-50 (400 mil)**

(Thin Small Outline, SMD)



1) Does not include plastic or metal protrusion of 0.25 max. per side